REMARKS

The Final Office Action mailed November 5, 2003, has been received and reviewed. Claims 3–6, 9, 10, 21–24, and 27–32 are currently pending in the application. The indication of allowable subject matter in each of claims 29–32 is noted with appreciation. Each of claims 3–6, 9, 10, 21–24, 27, and 28 stands rejected. Claim 1 is also cited in the outstanding Final Office Action as being rejected. *See, Final Office Action* at page 2, ¶ 2. However, claim 1 was canceled by way of the amendment filed August 15, 2003 and, accordingly, the rejection as to this claim is moot. Applicant proposes to amend each of claims 3–6, 9, 10, 21–24, and 27–32 as set forth hereinabove. Reconsideration of the application in light of the proposed amendments and the following remarks is respectfully requested.

Amendments to the Specification

It is proposed that paragraphs **[0006]** and **[0008]** be amended as set forth hereinabove to correct minor editorial problems. It is respectfully submitted that the amendments are supported by the as-filed specification and drawings and no new matter has been added. Please enter the paragraphs as amended.

35 U.S.C. § 103(a) Obviousness Rejections

A) Applicable Authority

The basic requirements of a *prima facie* case of obviousness are summarized in MPEP §2143 through §2143.03. In order "[t]o establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success [in combining the references]. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d

1438 (Fed. Cir. 1991)." MPEP §2143 (emphasis added). Further, in establishing a *prima facie* case of obviousness, the initial burden is placed on the Examiner. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985)." MPEP §2143. *See also*, MPEP §706.02(j).

B) Obviousness Rejection Based on U.S. Patent 6,124,189 to Watanabe et al. in View of U.S. Patent 6,479,899 to Fukuda et al.

Claims 3–6, 9, 10, 21–24, 27, and 28 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,124,189 to Watanabe et al. (hereinafter the "Watanabe reference") in view of U.S. Patent 6,479,899 to Fukuda et al. (hereinafter the "Fukuda reference"). Claim 1 was also cited as being included in this rejection. *See, Final Office Action* at page 2, ¶ 2(1). However, as previously set forth, claim 1 was canceled by way of the amendment filed August 15, 2003. Accordingly, the rejection as to this claim is moot.

As the Examiner has failed to establish a *prima facie* case of obviousness of claims 3–6, 9, 10, 21–24, 27, and 28 based upon the asserted combination of the Watanabe reference and the Fukuda reference, Applicant respectfully traverses this rejection, as hereinafter set forth.

Referring initially to independent claim 3, as proposed to be amended herein, it is respectfully submitted that the Watanabe reference in view of the Fukuda reference fails to teach or suggest all of the limitations recited in this claim. Independent claim 3, as proposed to be amended herein, recites a transistor for the dissipation of electrostatic discharges. The transistor comprises, in part, an intermediate structure comprising a substrate having at least one thick field oxide area and at least one active area including at least one implanted drain region and at least one implanted source region. The intermediate structure further includes at least one transistor gate member spanned between the at least one implanted drain region and the at least one implanted source region on the at least one active area. The transistor further comprises a first

barrier layer planarized down to the at least one transistor gate member and substantially covering the at least one thick field oxide area and the at least one active area, and adjacent the at least one transistor gate member. Still further, the transistor of independent claim 3, as proposed to be amended herein, comprises at least one drain contact plug and at least one source contact plug, each extending through the first barrier layer and in electrical communication with the at least one implanted drain region and the at least one implanted source region, respectively, on the substrate. The transistor further comprises an individual drain contact land disposed atop the at least one drain contact plug and a portion of the first barrier layer and an individual source contact land disposed atop the at least one source contact plug and a portion of the first barrier layer. The individual drain contact land is wider than the at least one drain contact plug and the individual source contact land is wider than the at least one source contact plug. A second barrier layer is disposed over the first barrier layer, the individual drain contact land, and the individual source contact land. *At least one upper source contact extends through the second barrier layer, the at least one upper source contact being in electrical communication with the individual source contact land,* ***and*** *at least one upper drain contact extends through the second barrier layer, the at least one upper drain contact being in electrical communication with the individual drain contact land.*

It is respectfully submitted that the Watanabe reference in view of the Fukuda reference fails to teach or suggest all of the limitations of independent claim 3, as proposed to be amended herein. More particularly, the Watanabe reference in view of the Fukuda reference fails to teach or suggest a transistor comprising, in part, at least one upper source contact extending through a second barrier layer, the at least one upper source contact being in electrical communication with an individual source contact land, ***and*** at least one upper drain contact extending through a second barrier layer, the at least one upper drain contact being in electrical communication with an individual drain contact land, as recited in independent claim 3, as proposed to be amended herein. As such, it is respectfully submitted that a *prima facie* case of the obviousness of independent claim 3, as proposed to be amended herein, cannot be established based upon the asserted combination of references.

By way of contrast, the Watanabe reference discloses a metal strapped polysilicon gate metallization structure for a semiconductor device and method of forming the same. *See, Watanabe reference* at Abstract; col. 2, lines 18–20. The metal strapped polysilicon gate structure of the Watanabe reference includes a p-type silicon substrate 100 having an active area which is isolated from other elements by shallow trench isolation regions 101. Spaced apart source/drain diffusion regions 107 are formed in the substrate and a gate structure 130 is insulatively spaced from a channel region between the source/drain regions 107 by a gate dielectric film 102. *See id.* at col. 3, lines 37–55. An insulating layer 108 is formed on the silicon substrate 100, the shallow trench isolation regions 101 and the source/drain regions 107. *See id.* at FIG. 7B; col. 5, line 65–col. 6, line 10. Contact openings 109 are formed in the insulating layer 108 and include a titanium/titanium nitride layer 110 on the sidewalls thereof. *See id.* at col. 6, lines 9–12. The contact openings 109 are filled with a conductive material layer 111C. A second insulating layer 112 is formed over the first insulating layer 108 and openings 113 are formed therein. The openings are filled with a conductive material to form wiring layer 114. *See id.* at FIG. 7B; col. 6, lines 15–20.

It is recognized in the outstanding Final Office Action that the Watanabe reference "does not expressly disclose an upper contact extending though [sic] a second barrier layer, said second barrier layer disposed over said first barrier layer, to form an electrical contact with said individual contact land." *See, Final Office Action* at page 2, ¶ 2(5). While Applicant agrees that the Watanabe reference does not disclose the described structure, it is noted that the structure described as delineating a deficiency in the Watanabe reference is ***not*** identical to the structure recited in independent claim 3, as proposed to be amended herein. Rather, as previously discussed, independent claim 3, as proposed to be amended herein, recites, in part, at least one upper source contact extending through a second barrier layer, the second barrier layer disposed over the first barrier layer, the at least one upper source contact being in electrical communication with the individual source contact land, ***and*** at least one upper drain contact extending through the second barrier layer, the at least one upper drain contact being in electrical communication with the individual drain contact land. Accordingly, independent claim 3, as

proposed to be amended herein, recites not only an upper contact extending through a second barrier layer, the second barrier layer disposed over a first barrier layer, as stated in the outstanding Final Office Action, but recites ***both*** an upper source contact ***and*** an upper drain contact, each of which extends through the second barrier layer. It is respectfully submitted that the Watanabe reference fails to teach or suggest this structure of independent claim 3, as proposed to be amended herein.

Applicant respectfully submits that the Fukuda reference also fails to teach or suggest the structure recited in independent claim 3, as proposed to be amended herein. Rather, the Fukuda reference discloses a memory cell structure, and method of making the same, in which a capacitor is formed in the uppermost layer of multiple, stacked metal wiring layers. *See, Fukuda reference* at col. 3, lines 48–56. In the memory cell structure of the Fukuda reference, a gate electrode 3 is formed in a first passivated insulating film layer 8, the gate electrode 3 spanning between diffusion layers 4 and 5 (*i.e.*, drain and source areas) on a silicon substrate 1. Contact plugs 9 are formed in the first passivated insulating film layer 8, one connected to each diffusion layer 4, 5. *See id.* at col. 1, line 27; col. 3, lines 48–56. A second insulating film 12 is then formed over the first insulating film layer 8 and the contact plugs 9. A connecting pad 10 is subsequently formed in the second insulating film 12 over one of the contact plugs 9 (*i.e.*, the contact plug connected to one of the diffusion layer 4 or 5) and a bit line 10' is formed in the second insulating film 12 over another of the contact plugs 9 (*i.e.*, the contact plug 9 connected to the other of the diffusion layers 4 or 5). *See id.* at col. 6, lines 14–38; FIG. 1. A plug 14, *e.g.*, a tungsten plug, is subsequently formed in the second insulating film 12 over the connecting pad 10. *See id.* While in the memory cell structure of the Fukuda reference, the diffusion layers 4, 5 are not specifically denoted as source or drain regions, it is noted that the gate electrode 3 spans between a source region and a drain region, as known to those of ordinary skill in the art, and as recited in independent claim 3 of the present application, as proposed to be amended herein.

In the memory cell structure of the Fukuda reference, a plug 14 is formed in the second insulating film 12 over ***only*** the connecting pad 10 and not over the bit line 10'. *See, Fukuda reference* at FIG. 1. Accordingly, the memory cell structure of the Fukuda reference discloses

either an upper source contact extending through the second insulating film and in electrical communication with a source connecting pad ***or*** an upper drain contact extending through the second barrier layer and in electrical communication with a drain connecting pad ***but not both***. It is stated in the outstanding Final Office Action that "[t]he fact that Fukuda does not expressly disclose the contact structure connected to the bit line does not make the reference faulty." *Final Office Action* at page 7, lines 1–4. It is further stated that the Fukuda reference discloses a contact structure that, if applied to the bit line contact of the structure disclosed by the Watanabe reference, would produce the claimed invention. *See id.* Applicant respectfully traverses this assertion.

It is respectfully submitted that the asserted combination of the Watanabe reference and the Fukuda reference fails to teach or suggest all of the limitations recited in independent claim 3, as proposed to be amended herein. As such, contrary to that asserted in the Final Office Action, if the contact structure of the Fukuda reference were to be applied to the bit line contact of the structure disclosed by the Watanabe reference, a structure having ***either*** an upper source contact extending through a second insulating film and in electrical communication with a source connecting pad, the second insulating film disposed over a first insulating film, ***or*** an upper drain contact extending through the second barrier layer and in electrical communication with a drain connecting pad ***but not both***.

It is further asserted in the Final Office Action that "[i]t would have been obvious for one skilled in the art at the time of the invention to improve upon the device of Watanabe in the manner of a more comprehensive interconnect structure as disclosed by Fukuda for the purpose, for example, of providing a multi-level interconnect structure that will provide greater device insulation of the device active region yet provide the desired conductivity of Fukuda to upper level devices." *Final Office Action* at page 2, ¶ 2(5), line 5–page 3, line 4. However, it is respectfully submitted that there is no suggestion or motivation, either in the Watanabe reference and/or the Fukuda reference, nor in the knowledge generally available to one of ordinary skill in the art, to modify the teachings of the cited references to achieve a transistor structure comprising, in part, at least one upper source contact extending through a second barrier layer,

the second barrier layer disposed over the first barrier layer, the at least one upper source contact being in electrical communication with the individual source contact land, **and** at least one upper drain contact extending through the second barrier layer, the at least one upper drain contact being in electrical communication with the individual drain contact land, as recited in independent claim 3, as proposed to be amended herein. Any such modification could only have been occasioned by improper use of hindsight provided by the teachings of the present application.

As neither the Watanabe reference nor the Fukuda reference, nor the combination thereof, teaches or suggests a transistor comprising, in part, at least one upper source contact extending through a second barrier layer, the at least one upper source contact being in electrical communication with an individual source contact land, ***and*** at least one upper drain contact extending through a second barrier layer, the at least one upper drain contact being in electrical communication with an individual drain contact land, as recited in independent claim 3, as proposed to be amended herein, it is respectfully submitted that a *prima facie* case of the obviousness of independent claim 3 cannot be established based upon the asserted combination of references. Accordingly, it is respectfully requested that the rejection under 35 U.S.C. § 103(a) of claim 3 based upon the asserted combination of the Watanabe and Fukuda references be withdrawn.

Each of claims 4–6, 9 and 10 depends directly from claim 3 and, thus, a *prima facie* case of obviousness based upon the asserted combination of references also cannot be established for these claims. *See, In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988) (dependent claims are nonobvious under 35 U.S.C. § 103(a) if the independent claims from which they depend are nonobvious). Thus, it is respectfully requested that the obviousness rejection of claims 4–6, 9 and 10 be withdrawn as well.

Independent claim 21, as proposed to be amended herein, recites a semiconductor device including at least one transistor for the dissipation of electrostatic discharges which includes similar structure to that recited in independent claim 3, as proposed to be amended herein. Accordingly, Applicant submits that a *prima facie* case of obviousness based upon the

combination of the Watanabe and Fukuda references cannot be established for claim 21 for at least the same reasons as those stated above with regard to claim 3. Additionally, each of claims 22–24, 27, and 28 depend directly from claim 21 and, thus, a *prima facie* case of obviousness based upon the asserted combination of references also cannot be established for these claims. *See, In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). Thus, it is respectfully requested that the obviousness rejection of claims 21–24, 27 and 28 be withdrawn as well.

Each of claims 3–6, 9, 10, 21–24, 27, and 28 are believed to be in condition for allowance and such favorable action is respectfully requested.

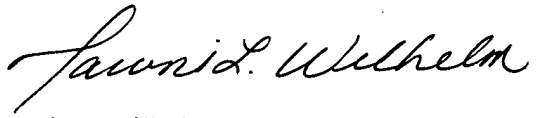
ENTRY OF AMENDMENTS

The proposed amendments to claims 3–6, 9, 10, 21–24, and 27–32 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. Further, the amendments do not raise new issues or require a further search. Finally, if the Examiner determines that the amendments do not place the application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

Claims 3–6, 9, 10, 21–24, and 27–32 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should it be determined that additional issues remain which might be resolved by a telephone conference, the Examiner is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,



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